REMARKS

Claims 1-18 are all of the pending claims, with claims 1 and 15 being written in independent form.

I. Drawings:

The Examiner objects to the drawings because the reference characters appearing in Figs. 1-9 are not legible. Applicant submits replacement Figs. 1-9 to address the Examiner's concerns. If the Examiner still believes that portions of the drawings are not legible, then he is respectfully requested to point out the alleged deficiency with more specificity to inform any further response that may be necessary.

II. Claim Rejections Under 35 USC §112(2nd):

The Examiner rejects claims 1-18 under 35 USC 112(2nd) for the reasons noted at numbered paragraph 3 of the Office Action. In response, Applicant amends in part and traverses in part.

The Examiner points out that the relationship between the "*input length*" and the "*code length*" (as defined in independent claims 1 and 15) is unclear. As a path of least resistance, and in view of the Examiner's helpful comments, Applicant amends independent claim 1 to recite that the analog decoder core has an input with "*an input length of bits that is less than the code length of bits.*" Applicant also amends independent claim 15 to recite that the code data has "*a code length of bits that is greater than the input length of bits.*" If the Examiner believes that any further changes are necessary, then the Examiner is invited to contact the undersigned to discuss the same.

Turning to the next point, the Examiner points out that because the decoder is set to receive code data having a code length, the code length must be the same as the input length of the decoder. Applicant respectfully disagrees.

Consider the example, non-limiting embodiment depicted in Figs. 1 and 2(a) – 2(c), which is discussed at paragraphs [0050]-[0067] of the instant specification. Here, the decoder has a total input length of W, which is only a fraction of code length of the

code data. From a functional standpoint, a portion of the code data may be loaded onto the decoder prior to each of a plurality of read operations. For example, as shown in Fig. 2(a), an initial portion (e.g., the first W bits) of the code data may be applied to the decoder, and an initial read operation may be performed.[1] Next, a second portion (e.g., the next W-2L bits) of the code data may be applied to the decoder, and a second read operation may be performed.[2] Such apply/read operations may continue until the end of the overall code data is reached. Fig. 2(c) depicts the decoding of the last window, where the end of the code data has been reached.[3] In summary, according to the example, non-limiting embodiments of the present invention, the code length is ***not*** the same as the input length of the decoder.

For at least the foregoing reasons, Applicant respectfully requests the Examiner to reconsider and withdraw the raised rejections under 35 USC §112(2nd).

III. Allowable Subject Matter:

At numbered paragraph 6 of the Office Action, the Examiner indicates that claims 2-14 and 16-18 would be allowable if they were rewritten in independent form and to overcome the 35 USC §112(2nd) rejections. Applicant believes that the §112(2nd) rejections have been appropriately addressed, but not rewrite any of the claims (as suggested by the Examiner) because independent claims 1 and 15 are believed to be patentable for the reasons discussed in detail below.

IV. Claim Rejection on Prior Art Grounds:

The Examiner rejects claims 1 and 15 under 35 U.S.C. §103(a) as being obvious over US 6,577,462 to Hamada et al. ("Hamada"). Applicant respectfully traverses this rejection in view of the following remarks.

The Examiner relies upon Hamada to teach or suggest each and every feature of the invention defined by claims 1 and 15. In so doing, the Examiner acknowledges that the reference fails to disclose (1) the application of a portion of the code data to the

[1] Spec., [0059]-[0061].
[2] Spec., [0062] and [0063].
[3] Spec., [0064]-[0067].

analog decoder and (2) the input of the analog decoder is less than the code length. Therefore, the Examiner points out that a conventional coding algorithm involves adding insert bits to the original input; hence, the length of the coded data will be greater than the input length of the decoder. Applicant respectfully submits that this rejection position is not convincing for the following reasons.

A. Independent Claim 1 – The Method:

The rejection position appears to be incorrect on its face. This is because independent claim 1 requires more than simply applying a portion of code data to an analog decoder core. Indeed, claim 1 recites applying a portion of code data ... "*prior to each of a plurality of read operations*." The Examiner's rejection position appears to simply gloss over this feature.

In any event, Hamada is not pertinent. With reference to Fig. 3 of Hamada (which is the embodiment asserted by the Examiner), the analog decoder circuit 22 decodes a signal when the sync control start signal 25 is activated.[4] The decoded data is inputted to the data conversion circuit 24. According to Hamada's straightforward disclosure, the data control circuit 7 inactivates the sync control start signal 25, when the analog decoder circuit 22 ***finishes*** the processing of the signal. That is, according to Hamada's straightforward disclosure, the code data in one sector (which resides between non-data gaps of a track) is decoded via a ***single*** apply/read operation. Certainly then, the reference is not pertinent to applying a portion of code data ... "*prior to each of a plurality of read operations*," as recited in claim 1.

Turning to the next point, the Examiner's allegations concerning ***coding*** techniques are simply not pertinent. This is because claim 1 is directed to a ***decoding*** method (not an encoder). More specifically, an encoder that adds insert bits to the code data (as alleged by the Examiner) may have nothing whatsoever to do with an input length of a decoder. Furthermore, the Examiner's remarks seem to intimate a belief that the input length of a encoder and the input length of an decoder must be the same. But this is not necessarily true. In any event, Applicant respectfully requests the

[4] Hamada, col. 6, lines 6+.

Examiner to cite a reference teaching a coding technique that involves adding insert bits and an associated decoder having an input length that is less than the code length. Otherwise, the rejection position appears to be based upon an impermissible hindsight of the instant specification.

B. Independent Claim 15 – The Apparatus:

Independent claim 15 is somewhat similar to claim 1 to the extent that claim 15 recites (among other things) that the code data has a code length of bits that is greater than the input length of bits of the analog decoder core input. Accordingly, independent claim 15 is believe to be patentable for reasons analogous to those noted above with respect to claim 1.

CONCLUSION

In view of the above, Applicant respectfully requests reconsideration and allowance of each of claims 1-18.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,
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AMENDMENTS TO THE DRAWINGS

The attached 7 sheets of drawings have been revised by improving the line quality (e.g., darkening the lines).

Attachments: 7 replacement sheets of drawings.